Remarks

In a case now pending before the Office for over ten (10) years, applicant can not help but feel misused by the process and believes that the stated final rejection in the Office Action dated February 27, 2007 crosses the boundary between persistent and cynicism.

To maintain a position that pending claims 25-28 and 30-34 are unpatentable under 35 U.S.C. § 103 over U.S. Patent No. 5,566,045 to Summerfelt et al. in view of U.S. Patent No. 5,254,217 to Maniar et al. is simply not credible. The addition of U.S. Patent No. 5,599,424 to Matsumoto et al. in this obviousness combination adds nothing of substance to the examination.

The Office admits (and remarkably quotes supporting citations) that Maniar expressly teaches away from exactly the result expressly recited in the pending claims.

Again, for the record on appeal, Maniar states:

> To complete the fabrication of capacitor 60, a *high resolution etch* process is ***required*** to define the first and second RuO2 layer and the intermediate PLZT layer. Capacitor ***must*** have the necessary geometric characteristics to be integrated into a complex semiconductor device such as a ultra-large-scale-integrated circuit. The fabrication of capacitor 60 ***requires*** that the etch process *not only be capable of high resolution, but also be* ***highly selective to underlying layers***. For example, it is required that the etching of the first RuO2 layer ***proceed to the interface between the first RuO2 layer and substrate 54 without unduly etching away the surface of substrate 54***.

(Maniar at Column 5, lines 19-31, emphasis added).

The examiner's rejection theory admits that an element recited in claims 25 and 30 (i.e., a lower substrate over etched to the point where a step is formed) is omitted from the primary reference, Summerfelt. To back-fill this omission, the examiner has cited Maniar. Yet, the ONLY RuO2 etch process proposed by Maniar is expressly intended to ***avoid etching*** **of the lower substrate**.

Undeterred by the actual description and clearly stated purpose of the etching process in Maniar, the examiner (perhaps taking official but un-noted notice?) concludes that Maniar can not possibly come to "a sudden screeching stop," but must somehow materially etch *some* portion of the substrate.

Applicant's first response to this assumption is, "So what?" Applicant has not claimed the "etching" (inadvertent or otherwise) of "some portion" of the lower substrate. Applicant does not present method claims here!

Applicant also objects to the improper "translation" of his expressly recited **structural limitation** in a device claim into some kind of hypothetical "process effect" element that MAY occur within the context of the examiner's hypothesis. This "language translation for ease of rejection approach" is particularly obnoxious since Maniar and Matsumoto expressly teach away for the process results hypothesized by the examiner. The teachings of Maniar, if anything, are actually reinforced by the noted discussion in Matsumoto. Here, Matsumoto's alleged improvement is one wherein "the silicon oxide layer 4 is never substantially etched as was the case in the conventional manufacturing method." (See, Matsumoto at Column 5, lines 54-59, emphasis added).

The examiner's entire theory is one of **assuming** imperfection (at some undefined level) in the application of the etching process disclosed in Maniar. In the mind of the examiner, this assumed imperfection in "coming to a sudden screeching halt" must exist, because Matsumoto alleges some reduction in the amount of lower substrate etching inadvertently done by an unspecified "conventional manufacturing method." Ergo, in the examiner's conclusion, because the very object and intent of the etching process disclosed in Maniar must fail, the fact that Maniar AND Matsumoto specifically teach away from the formation of the claimed invention means nothing.

Thus, the examiner opens a brave new front in the expansion of U.S. law related to obviousness determinations. It is apparently no longer necessary to consider the express teachings and clearly stated purposes of prior art references. No. So long as some question (no matter how unsupported by the evidence of record) may be raised regarding the actual implementation of a prior art technique, the Office may assume a directly contrary outcome and then postulate an obviousness rejection upon this assumption.

The examiner may not interpret claim language reciting "a step in an upper surface of the lower substrate" as meaning "inadvertently removing some of the lower substrate." The examiner may certainly not take this misinterpreted claim

language and then assume that the prior art must somehow fail at some material level in direct contradiction to its actual teachings. The examiner may most certainly not take the misinterpreted claim language, unsupported assumption regarding the prior art and reach an obviousness conclusion.

Reconsideration of pending claims is requested. If the examiner persists in his combination of the given references, applicant requests some further explanation of his reasoning so that a subsequent appeal may be fully responsive. Namely, if the primary reference fails to teach an etched lower substrate, and the two secondary references specifically teach selective etching processes that seek to avoid any substantial etching of the lower substrate, where does the examiner find suggestion in the combined art that teaches a lower substrate sufficiently etched to form an actual step?

Respectfully submitted,
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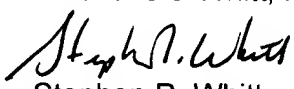

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